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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/917,195	07/26/2001	Song Xue	08305/100001/20-15	9616

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EXAMINER	
MISLEH, JUSTIN P	
ART UNIT	**PAPER NUMBER**
2612	

DATE MAILED: 09/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/917,195	XUE, SONG	
	Examiner	Art Unit	
	Justin P. Misleh	2612	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 June 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1- 14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 - 3, 7, 12, and 14* is/are rejected.

7)☐ Claim(s) *4 - 6, 8 - 11, and 13* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 June 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Note to Applicant: The Examiner of record for the present application has changed.

Response to Arguments

1. Applicant's arguments with respect to Claims 1 and 14 have been considered but are moot in view of the new grounds of rejection. However, the Examiner approves Applicant's drawing amendment to figure 5. There are no further objections to the specification.

Drawings

2. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) not mentioned in the description: 722 (figure 7).

Corrected drawing sheets in compliance with 37 CFR 1.121(d), or amendment to the specification to add the reference character(s) in the description in compliance with 37 CFR 1.121(b) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the Examiner, the Applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. **Claim 14** is rejected under 35 U.S.C. 102(b) as being anticipated by Tsang et al. (US 5 900 623).

5. For **Claim 14**, Tsang et al. disclose, as shown in figures 4 and 7 and as stated in columns 5 (lines 21 – 26), 10 (lines 11 – 24 and 31 – 38) and 13 (lines 42 – 48), a method, comprising:

increasing a level of an output reset signal to form a boosted level voltage, which is greater than a power supply voltage (see column 10, lines 11 – 24 and 31 – 38);

isolating said boosted level voltage (see explanation below); and

biasing said boosted level voltage to produce an output voltage which is related to an amount of said bias added to an amount of said power supply voltage (this is an inherent to forming "boosting level voltage, which is greater than a power supply voltage" as claimed above; also see explanation below).

Tsang et al. specifically states, in column 10 (lines 11 – 24), blooming is caused when the photosensitive region (photodiode PD) is forward-biased and to prevent blooming (anti-blooming) is it necessary to clamp the reversed-biased voltage across the photodiode so that it is no less than the gate-source voltage of charge transfer switches N1 and N2. In other words, a constant diode voltage is maintained across the photodiode (PD) during the integration period and at all other times, including a resetting period, the diode voltage is clamped to a reverse-

biased (positive) voltage to prevent blooming (see column 5, lines 21 – 26). Thus, the clamping provided by Tsang et al. directly corresponds to isolating the boosted level voltage so as to protect at least one transistor against being forward biased by said boosted reset voltage.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. **Claims 1, 2, 3, 7, and 12** are rejected under 35 U.S.C. 103(a) as being unpatentable over Tsang et al. (US 5 900 623) in view of Fujikura (US 5 949 271).

8. For **Claim 1**, Tsang et al. disclose, as shown in figures 4 and 7 and as stated in columns 5 (lines 21 – 26), 10 (lines 11 – 24 and 31 – 38) and 13 (lines 42 – 48), an image sensor, comprising:

a photosensitive region (photodiode PD);

a voltage boosting circuit (not specifically shown ; however, stated by Tsang et al. as being present), said voltage boosting circuit producing a boosted reset voltage on a reset line (ST) at a level higher than a power supply output voltage level (see column 10, lines 11 – 24 and 31 – 38); and

a voltage protection circuit (including photodiode PD and charge transfer transistors N1 and N2), said voltage protection circuit being connected to said reset line and protecting at least

one transistor (N1) against being forward biased by said boosted reset voltage (see explanation below).

Tsang et al. specifically states, in column 10 (lines 11 – 24), blooming is caused when the photosensitive region (photodiode PD) is forward-biased and to prevent blooming (anti-blooming) is it necessary to clamp the reversed-biased voltage across the photodiode so that it is no less than the gate-source voltage of charge transfer switches N1 and N2. In other words, a constant diode voltage is maintained across the photodiode (PD) during the integration period and at all other times, including a resetting period, the diode voltage is clamped to a reverse-biased (positive) voltage to prevent blooming (see column 5, lines 21 – 26). Thus, Tsang et al. in deed disclose a voltage protection circuit being connected to said reset line and protecting at least one transistor against being forward biased by said boosted reset voltage.

While Tsang et al. disclose a voltage boosting circuit (bootstrap circuit) for providing a boosted (bootstrapped) reset voltage higher than the power supply voltage, Tsang et al. do not disclose the particulars the voltage boosting circuit including a first capacitor and at least one switching element.

On the other hand, Fujikura also disclose a voltage boosting bootstrap circuit for an imaging device. More specifically, Fujikura discloses, as shown in figures 9 and 11 and as stated in columns 1 (lines 50 – 59), 3 (lines 33 – 49), 4 (lines 1 – 20 and 32 – 34), wherein the voltage boosting circuit is a bootstrap circuit providing a voltage level higher than a power supply voltage, wherein the bootstrap circuit comprises a first capacitor (Cb61) and at least one switching element (Tr61). Hence, Fujikura provides a voltage boosting circuit including a first capacitor and at least one switching element as recited.

As stated in column 1 (lines 35 – 42) of Fujikura, at the time the invention was made, it would have been obvious to one with ordinary skill in the art to have included a voltage boosting circuit including a first capacitor and at least one switching element as taught by Fujikura, in the imaging device including a boosted reset voltage disclosed by Tsang et al., for the advantage of increasing the bootstrapping effect without lowering the power source voltage or providing no reset transistor.

9. As for **Claim 2**, Tsang et al. disclose at least one additional transistor in the voltage protection circuit (N2). Furthermore, the voltage protection circuit (as explained above) device prevents the photodiode from blooming (caused by large currents from the voltage boosting circuit) by preventing the transistors in the voltage protection circuit (N1 and N2) from being forward-biased (see column 10, lines 11 – 24)

10. As for **Claim 3**, Fujikura discloses, as shown in figure 9, a first capacitor (Cb61), and first and second switching elements (Tr61 and Tr62, respectively), wherein said capacitor (Cb61) is first precharged at one plate by said first switching element (Tr61), and subsequently isolated at said one plate by said second switching element (Tr62), and biased at the other plate to produce an output voltage which is increased to a boosted voltage (Vdd plus bias) related to an amount of said bias added to an amount of the precharge.

11. As for **Claim 7**, Tsang et al. disclose an output switch (N2 – figure 4) which is capable of isolating against a voltage higher than a supply voltage. Tsang et al teaches that blooming occurs when a photodiode PD is momentarily forward biased (column 10, lines 11 – 24). To prevent blooming, Tsang et al teaches clamping the reverse-biased voltage across the photodiode

so that it is no less than a predetermined voltage. Therefore, switch (N2 – figure 4) is isolated against high voltage levels such that the photodiode (PD) is not forward biased.

12. As for **Claim 12**, Tsang et al. disclose an exemplary active pixel sensor (see figure 4) of a plurality of active pixel sensors comprising the image sensor, wherein each of the active pixels sensors include a row select transistor (N5), including a row select line, for selecting a row for output.

Allowable Subject Matter

13. **Claims 4 – 6, 8 – 11, and 13** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

14. The following is a statement of reasons for the indication of allowable subject matter:

While the closest prior art at least provides an image sensor with a voltage boosting circuit for producing a boosted reset voltage on a reset line such that the boosted reset voltage is a level higher than a power supply output voltage level and a voltage protection circuit that is connected to the reset line such that at least one transistor is protected against being forward biased by said boosted reset voltage; wherein the voltage boosting circuit is comprised of a first capacitor and first and second switching elements for the charging the capacitor;

The closest prior art does not teach or fairly suggest wherein a voltage that is greater than the power supply voltage does not forward bias the second switch element of the voltage boosting circuit or wherein the voltage boosting circuit comprises a second capacitor for producing a second output, a first passing transistor, and a second shorting transistor.

Additional Cited Prior Art

15. The prior art made of record and not relied upon is considered pertinent to Applicant's disclosure because each at least discloses an image sensing circuit having a boosted reset level voltage that is greater that a power supply voltage inputted into a boosting circuit for producing the boosted reset level (See Chen et al. and Imai et al.).

Conclusion

16. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

17. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Justin P Misleh whose telephone number is 571.272.7313. The Examiner can normally be reached on Monday through Friday from 8:00 AM to 5:00 PM.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Thai Q Tran can be reached on 571.272.7382. The fax phone number for the organization where this application or proceeding is assigned is 571.273.3000.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JPM
September 17, 2005